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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/597,306	07/19/2006	Yoshifumi Kanetaka	NEC 04P199	9113

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HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE, SUITE 140
TUCSON, AZ 85718

EXAMINER	
NORRIS, JEREMY C	

ART UNIT	PAPER NUMBER
2841	

NOTIFICATION DATE	DELIVERY MODE
12/29/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

admin@hayes-soloway.com
smckniff@hayes-soloway.com
nsoloway@hayes-soloway.com

Office Action Summary	Application No.	Applicant(s)	
	10/597,306	KANETAKA ET AL.	
	Examiner	Art Unit	
	Jeremy C. Norris	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings were received on 22 September 2009. These drawings are acceptable.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-3, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 11-219762 (Sony) in view of US 2004/0108130 A1 (Suzuki).

Sony discloses, referring primarily to figures 3 and 4, a circuit board (4) having a plurality of through holes (25) into which a plurality of leads (12) of an electronic device are inserted and soldered (14): wherein a volume of a through hole (25a) of said through holes, into which an outermost end lead of said leads of said electronic device is inserted, is larger than a volume of a through hole of said through holes, into which a lead of said leads, which is located at a position nearest to a center of said electronic device, is inserted. Sony does not specifically disclose using a lead-free solder wherein a conductive film is formed on a wall surface of said through holes [claim 1]. However, it is well known in the art to form holes in a circuit board with a conductive film on a wall surface and then solder a component into said hole with a lead free solder as evidenced by Suzuki (figure 6 and [0007]). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to provide a conductive film and lead-free solder to the invention of Sony as is known in the art and evidenced by Suzuki. The motivation for doing so would have been to ensure a reliable electormechanical connection.

Additionally, the modified invention of Sony teaches wherein a plane shape of each of said through holes is a circle, and wherein a diameter of said through hole, into which said outermost end lead of said electronic device is inserted, is larger than a

diameter of said through hole, into which said lead at the position nearest to the center of said electronic device is inserted [claim 2].

Regarding claim 3, modified Sony teaches the claimed invention as described above except Sony does not specifically teach that the diameter of said through hole, into which said outermost end lead of said electronic device is inserted, is not more than twice the diameter of said through hole, into which said lead at the position nearest to the center of said electronic device is inserted [claim 3]. However, it is well within the skill of the ordinary artisan to adjust the size of a hole of which fact the Examiner takes Official Notice. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the diameter of said through hole, into which said outermost end lead of said electronic device is inserted, is not more than twice the diameter of said through hole, into which said lead at the position nearest to the center of said electronic device is inserted in the modified invention of Sony as is known in the art. The motivation for doing so would have been to accommodate a lager pin that is not twice the diameter of the other pins.

Moreover, Sony discloses, a circuit board (24) having a plurality of through holes (25) into which a plurality of leads (12) of an electronic device (11) are inserted and soldered: wherein a size of a through hole (25a) of said through holes, into which an outermost end lead of said leads of said electronic device is inserted, the size being measured in a direction of a line that connects a position of said outermost end lead of said electronic device being mounted before being soldered and a center position of

said electronic device at a time of being mounted, is larger than a size of a through hole of said through holes, into which a lead of said leads which is located at the position nearest to the center of said electronic device is inserted, the size being measured in any direction in a plane. Sony does not specifically disclose using a lead-free solder wherein a conductive film is formed on a wall surface of said through holes [claim 5]. However, it is well known in the art to form holes in a circuit board with a conductive film on a wall surface and then solder a component into said hole with a lead free solder as evidenced by Suzuki (figure 6 and [0007]). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to provide a conductive film and lead-free solder to the invention of Sony as is known in the art and evidenced by Suzuki. The motivation for doing so would have been to ensure a reliable electormechanical connection.

Regarding claim 6, the limitation "wherein an opening of said through hole into which said outermost end lead of said electronic device is inserted is formed by drilling more than once or by moving a drill relative to the board." Is a process limitation in a product claim and thus has only been consider to the extent to which said process impacts the structure of said device, since it has been held "even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior

product was made by a different process. *In re Thorpe,* 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

Claims 1, 4, and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP Laid Open 12375/81 (Mitsumi) over Suzuki.

Mitsumi discloses referring primarily to figures 3 and 4, a circuit board (11) having a plurality of through holes (12) into which a plurality of leads (4) of an electronic device (3) are inserted: wherein a volume of a through hole (12d) of said through holes, into which an outermost end lead of said leads of said electronic device is inserted, is larger than a volume of a through hole of said through holes, into which a lead of said leads, which is located at a position nearest to a center of said electronic device, is inserted. Mitsumi does not specifically disclose that the leads are soldered with lead-free solder, wherein a conductive film is formed on a wall surface of said through holes [claim 1]. However, it is well known in the art to form holes in a circuit board with a conductive film on a wall surface and then solder a component into said hole with a lead free solder as evidenced by Suzuki (figure 6 and [0007]). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to provide a conductive film and lead-free solder to the invention of Mitsumi as is known in the art and evidenced by Suzuki. The motivation for doing so would have been to ensure a reliable electormechanical connection.

Moreover, Mitsumi discloses, a circuit board (11) having a plurality of through holes (12) into which a plurality of leads (4) of an electronic device (3) are inserted:

wherein a plane shape of a through hole of said through holes, into which a lead of said leads which is located at a position nearest to a center of said electronic device is inserted, is a circle, wherein a plane shape of a through hole of said through holes, into which an outermost end lead of said leads of said electronic device is inserted, is an ellipse having a major axis in a direction parallel with a line that connects a center of the corresponding through hole and a center position of said electronic device at a time of being mounted, and wherein a length of the major axis of said ellipse is longer than a diameter of said through hole, into which said lead at the position nearest to the center of said electronic device is inserted, and wherein the diameter of said through hole into which said lead at the position nearest to the center of said electronic device is inserted, is at least as long as a minor axis of said ellipse (figure 3). Mitsumi does not specifically disclose that the leads are soldered with lead-free solder, wherein a conductive film is formed on a wall surface of said through holes [claim 4]. However, it is well known in the art to form holes in a circuit board with a conductive film on a wall surface and then solder a component into said hole with a lead free solder as evidenced by Suzuki (figure 6 and [0007]). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to provide a conductive film and lead-free solder to the invention of Mitsumi as is known in the art and evidenced by Suzuki. The motivation for doing so would have been to ensure a reliable electormechanical connection.

Additionally, the modified invention of Mitsumi teaches wherein shapes of through holes (12b, 12c) of said through holes, which are located between said through hole (12a), into which said lead at the position nearest to the center of said electronic device is inserted, and said through hole (12d), into which said outermost end lead of said electronic device is inserted, are gradually changed from a shape of said through hole into which said lead at the position nearest to the center of said electronic device is inserted to a shape of said through hole into which said outermost end lead of said electronic device is inserted [claim 7] , wherein a center position of said through hole into which said outermost end lead of said electronic device is inserted is shifted in a direction away from a center position of said electronic device at the time of being mounted, from a position of said outermost end lead of said electronic device, which is mounted before being soldered, when a thermal expansion coefficient of said electronic device is larger than a thermal expansion coefficient of said circuit board, and the center position is shifted in a direction approaching a center of said electronic device at the time of being mounted, from a position of said outermost end lead of said electronic device, which is mounted before being soldered, when the thermal expansion coefficient of said electronic device is smaller than the thermal expansion coefficient of said circuit board (figure 4) [claim 8].

Similarly, Mitsumi discloses, a circuit board (11) having a plurality of through holes into which a plurality of leads (4) of an electronic device (3) are inserted: wherein a center position of a through hole (12d) of said through holes, into which an outermost end lead of said leads of said electronic device is inserted, is shifted in a direction away

from a center position of said electronic device at the time of being mounted, from a position of said outermost end lead of said electronic device, which is mounted before being soldered, when a thermal expansion coefficient of said electronic device is larger than a thermal expansion coefficient of said circuit board, and the center position is shifted in a direction approaching a center of said electronic device at a time of being mounted, from the position of said outermost end lead of said electronic device, which is mounted before being soldered, when the thermal expansion coefficient of said electronic device is smaller than the thermal expansion coefficient of said circuit board. Mitsumi does not specifically disclose that the leads are soldered with lead-free solder, wherein a conductive film is formed on a wall surface of said through holes [claim 9]. However, it is well known in the art to form holes in a circuit board with a conductive film on a wall surface and then solder a component into said hole with a lead free solder as evidenced by Suzuki (figure 6 and [0007]). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to provide a conductive film and lead-free solder to the invention of Mitsumi as is known in the art and evidenced by Suzuki. The motivation for doing so would have been to ensure a reliable electormechanical connection.

Response to Arguments

Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is (571)272-1932. The examiner can normally be reached on Monday - Thursday, 8:00 am - 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jinhee J. Lee can be reached on 571-272-1977. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeremy C. Norris
Primary Examiner
Art Unit 2841

/Jeremy C. Norris/
Primary Examiner, Art Unit 2841